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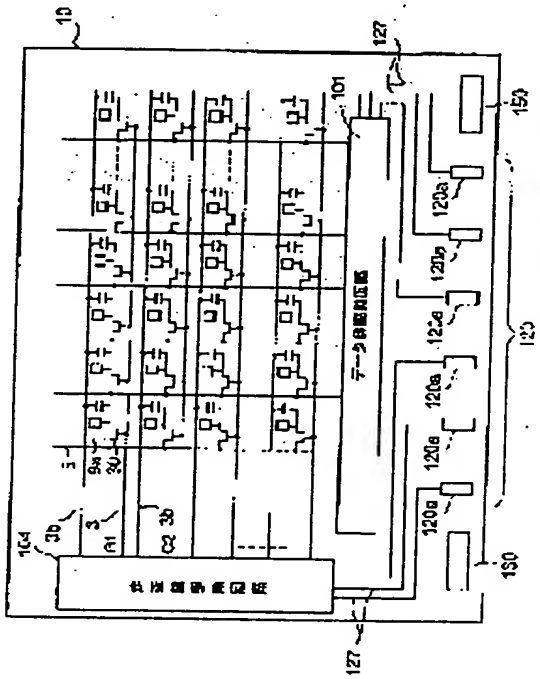
(54) METHOD FOR MANUFACTURING ELECTRODE SUBSTRATE, ELECTRODE SUBSTRATE AND OPTOELECTRONIC DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a test pattern which simplifies the measurement of the electrical characteristics of TFT.

SOLUTION: On a TFT array substrate 10 of a liquid crystal device, an N-channel TFT test pattern 130 and a P-channel TFT test pattern 140 are formed. Patterns of respective test patterns and a pad part are disposed, so that a same probe card is used for measuring the N-channel TFT test pattern 130 and the P-channel TFT test pattern 140.



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* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention belongs to the manufacture method of an electrode substrate, and belongs to the technical field of test pattern ** which measures the electrical property of the switching element especially formed on an electrode substrate.
[0002]
[Description of the Prior Art] Generally a switching element constitutes electro-optics equipment from an arranged electrode substrate. For example, between the TFT array substrates and opposite substrates which are an electrode substrate, a liquid crystal layer pinches the liquid crystal equipment as electro-optics equipment, and it is constituted.
[0003] The scanning line and the data line which cross mutually [this TFT array substrate / on a substrate] generally are arranged, and the switching element and the pixel electrode are formed for every intersection. Furthermore, in order to measure electrical properties, such as a switching element and a pixel electrode, on a substrate, the test pattern is arranged out of the viewing area.
[0004] The pattern for measuring the contact resistance in the pattern and contact hole for measuring the resistance of the pattern for measuring for example, a switching element property and the electric conduction film used for a pixel electrode etc. is arranged at this test pattern, and the electrical property of each element is measured using a prober.
[0005]
[Problem(s) to be Solved by the Invention] this invention makes it a technical problem to offer the manufacture method of an electrode substrate and an electrode substrate and electro-optics equipment which have the test pattern on which measurement using the above-mentioned test pattern is performed efficiently.
[0006]
[Means for Solving the Problem] In order to solve such a technical problem, this invention has adopted composition [like] as below.
[0007] The element by which the manufacture method of the electrode substrate of this invention has been arranged on a substrate and the aforementioned substrate, In the manufacture method of an electrode substrate of providing the 1st test pattern which is arranged on the aforementioned substrate and measures the electrical property of the aforementioned element, and the 2nd test pattern which is arranged on the aforementioned substrate and measures the electrical property of the aforementioned element The process which inspects the 1st test pattern of the above and the 2nd test pattern of the above with the same probe card, respectively is provided.
[0008] Since it can measure with a common probe card to two or more test patterns arranged on a substrate according to such composition of this invention, it has the effect that it can measure simply. Here, with an element, various elements called the semiconductor layer and gate electrode which constitute wiring, an electrode, a switching element, and a switching element, a contact hole, etc. are included.
[0009] Moreover, the aforementioned element has N type TFT and P type TFT, the 1st test pattern of the above is a test pattern which measures the electrical property of the aforementioned N type TFT, and the 2nd test pattern of the above is characterized by being the test pattern which measures the electrical property of the aforementioned P type TFT. Thus, a probe card can be communalized when

forming two or more transistors of a different mold.
[0010] Moreover, the 1st test pattern of the above and the 2nd test pattern of the above are characterized by having two or more pad sections arranged by the respectively same arrangement, and the aforementioned probe card having a probe needle corresponding to two or more aforementioned pad sections. The probe needle used by the 1st test pattern and the probe needle used by the 2nd test pattern can be communalized.
[0011] The 1st test pattern which has two or more pad sections which the electrode substrate of this invention is arranged on the element arranged on a substrate and the aforementioned substrate, and the aforementioned substrate, and measure the electrical property of the aforementioned element, In the electrode substrate possessing the 2nd test pattern which has two or more pad sections which are arranged on the aforementioned substrate and measure the electrical property of the aforementioned element Two or more pad sections of the 1st test pattern of the above and each 2nd test pattern of the above are arranged, and it is characterized by the bird clapper so that a common probe card may be used for the aforementioned measurement of the 1st test pattern of the above, and each 2nd test pattern of the above.
[0012] Since it can measure with a common probe card to two or more test patterns which can measure the property of the element indirectly formed on a substrate by measuring a test pattern, and are arranged on a substrate according to such composition of this invention, it has the effect that it can measure simply. Here, with an element, various elements called the semiconductor layer and gate electrode which constitute wiring, an electrode, a switching element, and a switching element, a contact hole, etc. are included.
[0013] Moreover, it is characterized by arrangement of two or more pad sections of the 1st test pattern of the above and each 2nd test pattern of the above being the same.
[0014] Moreover, the aforementioned element has N type TFT and P type TFT, the 1st test pattern of the above is a test pattern which measures the electrical property of the aforementioned N type TFT, and the 2nd test pattern of the above is characterized by being the test pattern which measures the electrical property of the aforementioned P type TFT. Thus, a probe card can be communalized when forming two or more transistors of a different mold.
[0015] The electrode substrate of this invention is characterized by being manufactured by **** by the manufacture method of the electrode substrate a publication. According to such composition, the property of the element of an effective field can be indirectly measured by the test pattern. For this reason, the high electrode substrate of quality can be obtained, without contacting a direct probe needle for the element in an effective field, and, for example, damaging an element with a probe needle accidentally for it.
[0016] The electro-optics equipment of this invention is characterized by having the electrode substrate of a publication in ****. Since the electro-optics equipment with which the electrode substrate judged to be an excellent article by measurement by the test pattern was used can be obtained according to such composition, the high electro-optics equipment of display grace can be obtained.
[0017]
[Embodiments of the Invention] Hereafter, the liquid crystal equipment as electro-optics equipment with which the TFT array substrate as an electrode substrate was incorporated in the operation gestalt of this invention is mentioned as an example, and is explained based on a drawing.
[0018] First, the composition of liquid crystal equipment is explained with reference to drawing 1 and drawing 2 . Drawing 1 is drawing showing equal circuits, such as various elements in two or more pixels formed in the shape of [which constitutes the viewing area of liquid crystal equipment] a matrix, and wiring, and a circumference drive circuit field. Drawing 2 is drawing of longitudinal section showing a part of viewing area of liquid crystal equipment, and circumference drive circuit field. In addition, in order to make each class and each part material into the size of the grade which can be recognized on a drawing, scales are made to have differed for each class or every each part material in each drawing.
[0019] As shown in drawing 1 , the TFT array substrate 10 as an electrode substrate which constitutes some liquid crystal equipments consists of circumference drive circuit fields which adjoin a viewing area and this viewing area and are arranged.

[0020] Pixel electrode 9a arranged in the shape of a matrix for every intersection of capacity line 3b and the scanning line 3 which have been arranged in parallel, the data line 6 arranged by intersecting the scanning line 3, and the these scanning lines 3 and the data line 6, and TFT (TFT is called hereafter) 30 as a switching element for controlling pixel electrode 9a are arranged at a viewing area. The source field of TFT30 was electrically connected to the data line 6 to which a picture signal is supplied, and the gate field of TFT30 has connected with the scanning line 3 to which a scanning signal is supplied electrically.

[0021] In the circumference drive circuit field, the scanning-line drive circuit 104 and the data-line drive circuit 101 are arranged, the scanning-line drive circuit 104 supplies a scanning-line signal to the scanning line 3, and the data-line drive circuit 101 supplies the picture signal to the data line 6.

[0022] The scanning-line drive circuit 104 impresses a scanning signal to the scanning line 3 by line sequential in pulse to predetermined timing based on the power supply supplied from the power circuit which is an external-control circuit, the reference clock supplied from the control-system circuit which is an external-control circuit, its reversal clock, etc.

[0023] Moreover, the data-line drive circuit 101 consists of a sampling circuit, a shift register, and a precharge circuit. A sampling circuit carries out the work which writes a picture signal at a time in the one data line, and the shift resist is carrying out the work which controls the timing of this sampling circuit of operation. A precharge circuit driving signal is supplied from an external-control circuit so that a precharge circuit may write in a precharge signal to the timing preceded with supply of a picture signal about each data line 6. A sampling circuit will sample these, if the picture signal supplied from a picture signal circuit 152 is inputted. That is, an input of a sampling circuit driving signal impresses a picture signal to the data line 6 one by one. With this operation gestalt, the complementary-type transistor structure in which high-speed operation is possible is adopted as a circuit of a shift resist. This complementary transistor consists of a P type transistor and an N type transistor.

[0024] And the terminal block 120 which is from two or more terminal area 120a electrically connected to the scanning-line drive circuit 104 and the data-line drive circuit 101 by wiring 127, respectively on the one-side side of a substrate is arranged. The test pattern 130 for N type transistors as the 1st test pattern and the test pattern 140 for P type transistors as the 2nd test pattern are arranged at the both sides of a terminal block 120 so that this terminal block 120 may be inserted. Moreover, after the measurement which used the test pattern, these test patterns could cut the substrate, could remove this portion, and may leave it as it is. In addition, about these test patterns 130 and 140, it mentions later.

[0025] As shown in the cross section of drawing 2 , liquid crystal equipment 200 is equipped with the liquid crystal layer 50 between the TFT array substrate 10 and the opposite substrate 20 by which opposite arrangement is carried out at this. In addition, in drawing 2 , as a circumference drive circuit field, the portion of the structure of a complementary transistor used for a shift register is mentioned as an example, and is explained.

[0026] TFT (following, TFT) 30 as a switching element which carries out switching control of each pixel electrode 9a is formed in the position which adjoins on the substrate 210 which consists of a quartz at each pixel electrode 9a at the TFT array substrate 10 in a viewing area. In the position which counters TFT30 respectively, shading film 11a is prepared between the TFT array substrate 10 and each TFT30. Shading film 11a consists of a metal simple substance containing at least one of Ti, Cr, W, Ta, Mo, and Pb(s) which are a desirable opaque refractory metal, an alloy, metal silicide, etc. If constituted from such a material, shading film 11a is destroyed by high temperature processing in the formation process of TFT30 for pixel switching performed after the formation process of shading film 11a on the TFT array substrate 10, or it can avoid fusing by it.

[0027] Furthermore, the ground insulator layer 12 is formed between shading film 11a and two or more TFT30. The ground insulator layer 12 is formed in order to carry out the electric insulation of the semiconductor layer 1a which constitutes TFT30 from shading film 11a. Furthermore, the ground insulator layer 12 also has a function as a ground film for TFT30 for pixel switching by being formed all over the TFT array substrate 10. The ground insulator layer 12 consists of high insulation glass, such as NSG (non doped silicate glass), or a silicon-oxide film, a silicon nitride film, etc.

[0028] TFT30 has semiconductor layer 1a and gate electrode 3a arranged on the wrap gate insulator

layer 2 and the gate insulator layer 2 in this corresponding to channel field 1a' of semiconductor layer 1a. TFT30 has the P type TFT structure where for example, B (boron) ion was injected into the semiconductor layer as an impurity, and was formed, and has LDD structure. The impurity ion by which semiconductor layer 1a has been arranged so that it may face across these fields further with low concentration source field 1b of low concentration [ion / impurity / by which it has been arranged at both sides so that it may face across this channel field / channel field 1a' and], and low concentration drain field 1c consists of 1d of high-concentration high concentration source fields, and high concentration drain field 1e.

[0029] On the gate insulator layer, gate electrode 3a which is a part of scanning line 3 and scanning line 3 which consists of doped polysilicon, and capacity line 3b are arranged. And an insulator layer 81 is arranged between the 1st layer so that these scanning lines 3, gate electrode 3a, and capacity line 3b may be covered, and the relay layer 80 which consists of tungsten silicide (WSi) is further arranged on the insulator layer 81 between the 1st layer. Capacity line 3b is electrically connected with shading film 11a through the contact hole 13 formed in the ground insulator layer 12, the gate insulator layer 2, and the insulator layer 81 between the 1st layer.

[0030] And the semiconductor layer which installed semiconductor layer 1a from high concentration drain field 1e is used as 1f of storage-capacitance electrodes, and 1st storage-capacitance 70a is formed by intervening the gate insulator layer 2 among these storage-capacitance electrodes by using as a storage-capacitance electrode a part of capacity line 3b which counters this. Furthermore, 2nd storage-capacitance 70b is formed by using a part of capacity line 3b and above-mentioned relay layer 80 which counters as a storage-capacitance electrode, and forming an insulator layer 81 in inter-electrode [these] between the 1st layer. And parallel connection of these [1st] and the 2nd storage capacitance 70a and 70b is carried out through contact hole 8a, and the storage capacitance 70 is formed.

[0031] Furthermore, the relay layer 80 is covered and an insulator layer 4 is arranged between the 2nd layer on an insulator layer 81 between the 1st layer. The data line 6 formed by intersecting the scanning line 3 on the insulator layer 4 between the 2nd layer is arranged. the data line 6 -- aluminum etc. -- low -- it consists of shading nature and conductive thin films, such as metal membrane metallurgy group silicide [****], and constitutes from aluminum here [, such as an alloy film,] The data line 6 is electrically connected with 1d of high concentration source fields through the contact hole 4 formed in the gate insulator layer 2, the insulator layer 81 between the 1st layer, and the insulator layer 4 between the 2nd layer. Between the 2nd layer containing the data line 6, an insulator layer 7 is arranged between the 3rd layer, and pixel electrode 9a which consists of ITO (Indium Tin Oxide) is arranged on the insulator layer 7 between the 3rd layer at the insulator layer 4 top.

[0032] One to which it corresponds of two or more pixel electrode 9a relays the relay layer 80 to high concentration drain field 1e, and it is connected to it. High concentration drain field 1e is electrically connected with the relay layer 80 through contact hole 8a formed in the gate insulator layer 2 and the insulator layer 81 between the 1st layer. Furthermore, the relay layer 80 and pixel electrode 9a are electrically connected through contact hole 8b formed in the insulator layer 4 and the insulator layer 7 between the 3rd layer between the 2nd layer.

[0033] On the insulator layer, the orientation film 16 which consists of a polyimide is arranged between the 3rd layer containing pixel electrode 9a.

[0034] On the other hand, the complementary transistor which becomes the TFT array substrate 10 in a circumference drive circuit field from the P type transistor (henceforth, P channel TFT) 140 and the N type transistor (henceforth, N channel TFT) 160 is arranged. Between this complementary transistor and the quartz substrate 210, the same ground insulator layer 12 as the ground insulator layer 12 in a viewing area is arranged in this layer.

[0035] Like TFT30 in a viewing area, B ion is poured in as an impurity, P channel TFT140 is manufactured, for example, P ion is poured in as an impurity, and N channel TFT160 is manufactured.

[0036] Such P channel TFT140 and N channel TFT160 have LDD structure, respectively, and the semiconductor 141 of P channel TFT140 consists of low concentration source field 141b of low concentration [ion / impurity / channel field 141a and / which has been arranged at both sides so that

it may face across this channel field] and low concentration drain field 141c, and 141d of high concentration source fields of high concentration / ion / impurity / by which it has been arranged so that it may face across these fields further] and high concentration drain field 141e. Moreover, the semiconductor 161 of N channel TFT160 consists of low concentration source field 161b of low concentration [ion / impurity / channel field 161a and / which has been arranged at both sides so that it may face across this channel field] and low concentration drain field 161c, and 161d of high concentration source fields of high concentration / ion / impurity / by which it has been arranged so that it may face across these fields further] and high concentration drain field 161e.

[0037] On channel field 141a of each semiconductor layer, and 161b, the gate electrodes 142 and 162 are arranged through the gate insulator layer 2 which covered the semiconductor layers 141 and 161 and has been arranged. These gate electrodes 142 and 162 are formed in gate electrode 3a of TFT30 in a viewing area, and this layer. Furthermore, these gate electrodes 142 and 162 are covered, and the insulator layer 81 and the insulator layer 4 between the 2nd layer are arranged between the 1st layer on the gate insulator layer 2. On the insulator layer 4, the source 143 and the drain 144 corresponding to P channel TFT140 are formed in the data gland 6 and this layer in a viewing area between the 2nd layer. The source 143 and the drain 144 are electrically connected to 141d of high concentration source fields, and high concentration drain field 141e through contact holes 145 and 146, respectively. Moreover, on the insulator layer 4, the source 163 and the drain 164 corresponding to N channel TFT160 are also formed in the data gland 6 and this layer in a viewing area between the 2nd layer. The source 163 and the drain 164 are electrically connected to 161d of high concentration source fields, and high concentration drain field 161e through contact holes 165 and 166, respectively.

[0038] Furthermore, these sources 143 and 163 and drains 144 and 164 are covered, and the insulator layer 7 is arranged between the 3rd layer.

[0039] On the other hand, the orientation film 22 which crosses all over the on a glass substrate 220, and consists of a counterelectrode 21 and a polyimide is formed one by one, and the opposite substrate 20 is constituted. A counterelectrode 21 consists of transparent conductivity thin films, such as ITO. Moreover, the shading film 23 is formed in the non-opening field of each pixel.

[0040] Next, the test pattern 130 for N type transistors as the 1st test pattern (henceforth, N channel test pattern) and the test pattern 150 for P type transistors as the 2nd test pattern (henceforth, P channel test pattern) which were mentioned above are explained using drawing 3 - drawing 9 .

[0041] Drawing 3 is the enlarged view of an N channel TFT test pattern, and drawing 4 is the enlarged view of a P channel TFT test pattern. Drawing 5 is the perspective diagram of the probe card used in common with the time of measurement of each test pattern. Drawing 6 is the enlarged view of the field A surrounded by the dotted line of the shape of a rectangle of drawing 3 , and drawing 7 is the enlarged view of the field B surrounded by the dotted line of the shape of a rectangle of drawing 4 . Drawing 8 is the enlarged view of the field D surrounded by the dotted line of the shape of a rectangle of drawing 3 , and drawing 9 is the enlarged view of the field E surrounded by the dotted line of the shape of a rectangle of drawing 4 .

[0042] An N channel TFT test pattern and a P channel TFT test pattern are formed simultaneously with formation of various elements, such as TFT in the viewing area mentioned above, and TFT in a pixel electrode and a circumference drive circuit field, respectively.

[0043] As shown in drawing 3 , the N channel TFT test pattern 130 has two or more pad sections 131-139, and as shown in drawing 4 , the P channel TFT test pattern 150 has two or more pad sections 151-159. As shown in drawing 3 and drawing 4 , arrangement of two or more pad sections of a P channel TFT test pattern and each N channel TFT test pattern has become the same, and the pad sections 131-139, and 151-159 are formed simultaneously with the pixel electrode in an above-mentioned viewing area. In addition, although the pad section is formed from the same ITO as a pixel electrode here in order to make structure intelligible, it is good also as redundant structure to which the aluminum layer and the ITO layer were electrically connected by the contact hole which the laminating of the aluminum and ITO which consist of the data line and this layer was carried out through the insulator layer for the reduction in resistance of the pad itself, and was formed into the insulator layer. Furthermore, the tungsten silicide layer which consists of a barrier layer mentioned above and this layer is also good also as a pad of structure which carried out the laminating, carried

out the laminating of the three layers, an aluminum layer, a tungsten silicide layer, and an ITO layer, and connected each electrically.

[0044] Moreover, drawing 5 is the perspective diagram of the probe card 170 used common to measurement of a P channel TFT test pattern and each N channel TFT test pattern. As a probe card 170 is attached in the prober which is a measuring device and it is shown in drawing 5 , it has two or more probe needles 172-179, a probe needle is contacted in the pad section, and measurement is performed.

[0045] The probe needles 171-174 arranged to the field of the rectangle C surrounded by the dotted line of a probe card 170 correspond to the pad sections 151-154 arranged to the field of the rectangle B surrounded by the dotted line of the pad sections 131-134 arranged to the field of the rectangle A surrounded by the dotted line of the N channel TFT test pattern 130 of drawing 3 , and the P channel TFT test pattern 150 of drawing 4 . That is, the probe needle 171 contacts at the pad section 131 or the pad section 151 at the time of measurement, the probe needle 172 contacts the pad section 132 or the pad section 152, the probe needle 173 contacts the pad section 133 or the pad section 153, and the probe needle 174 contacts the pad section 134 or the pad section 154 at it.

[0046] The probe needles 175-179 arranged to the field of the rectangle F surrounded by the dotted line of a probe card 170 correspond to the pad sections 155-159 arranged to the field of the rectangle E surrounded by the dotted line of the pad sections 135-139 arranged to the field of the rectangle D surrounded by the dotted line of the N channel TFT test pattern 130 of drawing 3 , and the P channel TFT test pattern 150 of drawing 4 . That is, the probe needle 176 contacts the pad section 136 or the pad section 156, the probe needle 177 contacts the pad section 137 or the pad section 157, the probe needle 175 pad section 135 or the pad section 155 is contacted at the time of measurement, and the probe needle 179 contacts [the probe needle 178 contacts the pad section 138 or the pad section 158, and] the pad section 139 or the pad section 159.

[0047] Next, the structure of a N channel each TFT test pattern and a P channel TFT test pattern is explained using drawing 6 - drawing 8 .

[0048] Drawing 6 is the enlarged view of the field surrounded by the rectangle A of the N channel TFT test pattern 130 of drawing 3 , and drawing 7 is the enlarged view of the field surrounded by the rectangle B of the P channel TFT test pattern 150 of drawing 4 .

[0049] Drawing 8 is the enlarged view of the field surrounded by the rectangle D of the N channel TFT test pattern 130 of drawing 3 , and drawing 7 is the enlarged view of the field surrounded by the rectangle E of the P channel TFT test pattern 150 of drawing 4 .

[0050] As shown in drawing 6 , in the field surrounded by the rectangle A of the N channel TFT test pattern 130 The pattern which measures contact resistance with capacity line 3b in a viewing area, and shading film 11a, The pattern which measures the electric resistance of the high concentration impurity ranges 161d and 161e of the semiconductor layer 161 of N channel TFT160 in a circumference drive circuit field, The pattern which measures the electric resistance of the low concentration impurity ranges 161b and 161c of the semiconductor layer 161 of N channel TFT160 in a circumference drive circuit field is arranged.

[0051] The pattern which measures contact resistance with capacity line 3b in a viewing area, and shading film 11a The pad section 131, the pad section 134, the doped polysilicon wiring 230a and 230b formed in this layer simultaneously with capacity line 3b, It consists of a gate insulator layer 2 which intervened between the shading layer 231, and the doped polysilicon wiring 230 and the shading layer 231 which were formed in this layer simultaneously with shading film 11a, and an insulator layer 81 between the 1st layer. That is, the doped polysilicon wiring 230a and 230b is electrically connected to the pad section 131 and the pad 134 through contact holes 400 and 401, respectively. Furthermore, the doped polysilicon wiring 230a and 230b is electrically connected with the shading layer 231 through the contact hole 405 formed in the gate insulator layer 2 and the insulator layer 81 between the 1st layer. In measurement, contact resistance with capacity line 3b in a viewing area and shading film 11a can be indirectly measured by contacting a probe needle to each of the pad sections 131 and 134, applying voltage, measuring current, and converting into resistance.

[0052] The pattern which measures the electric resistance of the high concentration impurity ranges 161d and 161e of the semiconductor layer 161 of N channel TFT160 in a circumference drive circuit

field consists of the pad section 133, the pad section 134, and a semiconductor layer 232 that the same high concentration impurity as the high concentration impurity ranges 161d and 161e of the semiconductor layer 161 contained. The semiconductor layer 232 is electrically connected with contact holes 402 and 404 with the pad sections 133 and 134, respectively. In measurement, the electric resistance of the high concentration impurity ranges 161d and 161e of the semiconductor layer 161 of N channel TFT160 in a circumference drive circuit field can be indirectly measured by contacting a probe needle to each of the pad sections 133 and 134, applying voltage, measuring current, and converting into resistance.

[0053] The pattern which measures the electric resistance of the low concentration impurity ranges 161b and 161c of the semiconductor layer 161 of N channel TFT160 in a circumference drive circuit field consists of the pad section 132, the pad section 134, and a semiconductor layer 233 that the same low concentration impurity as the high concentration low **** fields 161b and 161c of the semiconductor layer 161 contained. The semiconductor layer 233 is connected with the semiconductor layer 232, the field which laps with the pad sections 132 and 134 is a field (double slash upward slanting to the right) which the high concentration impurity contained, and the semiconductor layer 233 between the pad section 132 and the pad section 134 serves as a field (slash upward slanting to the right) which the low concentration impurity contained. The semiconductor layer 233 is electrically connected with the pad sections 132 and 134 by contact holes 403 and 404. In measurement, the electric resistance of the low concentration impurity ranges 161b and 161c of the semiconductor layer 161 of N channel TFT160 in a circumference drive circuit field can be indirectly measured by contacting a probe needle to each of the pad sections 132 and 134, applying voltage, measuring current, and converting into resistance.

[0054] Above, a probe needle is applied simultaneously, voltage is applied to each pad section one by one, current is read in the four pad sections 131-134, and resistance is converted into them.

[0055] On the other hand, as shown in drawing 7 , in the field surrounded by the rectangle B of the P channel TFT test pattern 150 141d of high concentration impurity ranges of the semiconductor layer 141 of the pattern which measures the electric resistance of the ground insulator layer 12, and P channel TFT140 in a circumference drive circuit field, The pattern which measures the electric resistance of the high concentration impurity ranges 1d and 1e of the semiconductor layer 1 of TFT30 in 141e and a viewing area, The pattern which measures the electric resistance of the low concentration impurity ranges 141b and 141c of the semiconductor layer 141 of P channel TFT140 in a circumference drive circuit field and the low concentration impurity ranges 1b and 1c of the semiconductor layer 1 of TFT30 in a viewing area is arranged.

[0056] The pattern which measures the electric resistance of the ground insulator layer 12 consists of the pad section 151, the pad section 154, a ground insulator layer 12, and an insulator layer 240 of this layer. The ground insulator layer 12 is electrically connected with the pad sections 151 and 154 through contact holes 410 and 411, respectively. In measurement, the electric resistance of the ground insulator layer 12 can be measured by contacting a probe needle to each of the pad sections 151 and 154, applying voltage, measuring current, and converting into resistance.

[0057] The pattern which measures the electric resistance of the high concentration impurity ranges 141d and 141e of the semiconductor layer 141 of P channel TFT140 in a circumference drive circuit field and the high concentration impurity ranges 1d and 1e of the semiconductor layer 1 of TFT30 in a viewing area consists of the pad section 153, the pad section 154, and a semiconductor layer 241 that the same high concentration impurity as the high concentration impurity ranges 141d, 141e, 1d, and 1e of the semiconductor layers 141 and 1 contained. The semiconductor layer 241 is electrically connected with contact holes 412 and 414 with the pad sections 153 and 154, respectively. In measurement, the electric resistance of the high concentration impurity ranges 141d and 141e of P channel TFT160 in a circumference drive circuit field and the high concentration impurity ranges 1d and 1e of TFT30 in a viewing area can be indirectly measured by contacting a probe needle to each of the pad sections 153 and 154, applying voltage, measuring current, and converting into resistance.

[0058] Low concentration impurity-range 141b of the semiconductor layer 141 of P channel TFT140 in a circumference drive circuit field, The pattern which measures the electric resistance of the low concentration impurity ranges 1b and 1c of the semiconductor layer 1 of TFT30 in 141c and a

viewing area It consists of the pad section 152, the pad section 154, and a semiconductor layer 242 that the same low concentration impurity as the low concentration low **** fields 141b and 141c of the semiconductor layer 141 and the low concentration impurity ranges 1b and 1c of the semiconductor layer 1 contained. The semiconductor layer 242 is connected with the semiconductor layer 241, the field which laps with the pad sections 152 and 154 is a field which the high concentration impurity contained, and the semiconductor layer 242 between the pad section 152 and the pad section 154 serves as a field which the low concentration impurity contained. The semiconductor layer 242 is electrically connected with the pad sections 152 and 154 by contact holes 413 and 414. In measurement, the electric resistance of the low concentration impurity ranges 141b and 141c in a circumference drive circuit field and the low concentration impurity ranges 1b and 1c in a viewing area can be indirectly measured by contacting a probe needle to each of the pad sections 152 and 154, applying voltage, measuring current, and converting into resistance.

[0059] A probe needle is applied simultaneously, voltage is applied to each pad section one by one, current is read in the four pad sections 151-154, and resistance is converted into them. As mentioned above, as shown in drawing 6 and drawing 7 , the test pattern and the pad are arranged so that the probe card with which each test pattern is used at the time of the measurement in each test pattern may become common.

[0060] As shown in drawing 8 , in the field surrounded by the rectangle D of the N channel TFT test pattern 130, the pattern which measures the TFT property of TFT of the sampling circuit in a circumference drive circuit field, and the pattern which measures the TFT property of N channel TFT160 of the shift register in a circumference drive circuit field are arranged.

[0061] The pattern which measures the TFT property of TFT of the sampling circuit in a circumference drive circuit field The source 251 formed in the same layer as the pad section 135, the pad section 136, the pad section 137, the gate electrode 253 formed in the same layer as the gate electrode of TFT of a sampling circuit, the source electrode of TFT of a sampling circuit, and a drain electrode And a drain 250, and the semiconductor layer of TFT of a sampling circuit and the semiconductor layer 252 of this layer, It consists of insulator layers 4 between the 2nd layer which intervenes between the gate insulator layer 2 which intervenes between the semiconductor layer 252 and the gate electrode 253 and the insulator layer 81 between the 1st layer, and the gate electrode 253, the source 251 and a drain 250. As shown in drawing 8 , the pad section 135 is electrically connected through the drain 250 and the contact hole 420. The pad section 136 is electrically connected through the source 251 and the contact hole 428. The pad section 137 is electrically connected with the gate electrode 253. The semiconductor layer 252 consists of a channel field, and the source field and drain field which have been arranged across a channel field. The gate insulator layer 2 is arranged so that the semiconductor layer 252 may be covered, the gate electrode 253 is arranged on the gate insulator layer 2, and TFT429 is formed. Semiconductor layer 252 portion which overlaps the gate electrode 253 superficially functions as a channel field. The drain field of the semiconductor layer 252 is electrically connected with the drain 250 through the contact hole 422. The source field of the semiconductor layer 252 is electrically connected with the source 251 through the contact hole 423. In measurement, a probe needle is contacted in the pad sections 135, 136, and 137 at each. By impressing voltage to the pad section 137, the TFT property of TFT429 can be measured by turning on switching of TFT429, applying voltage to the pad sections 135 and 136, measuring current, and converting into resistance. Thereby, the TFT property of a sampling circuit can be measured indirectly.

[0062] The pattern which measures the TFT property of N channel TFT160 of the shift register in a circumference drive circuit field The source 255 formed in the same layer as the pad section 138, the pad section 137, the pad section 139, the gate electrode 253, the source electrode of N channel TFT160 of a shift resist, and a drain electrode and a drain 254, and the semiconductor layer of TFT of a shift resist and the semiconductor layer 256 of this layer, It consists of insulator layers 4 between the 2nd layer which intervenes between the gate insulator layer 2 which intervenes between the semiconductor layer 256 and the gate electrode 253 and the insulator layer 81 between the 1st layer, and the gate electrode 253, the source 255 and a drain 254. As shown in drawing 8 , the pad section 138 is electrically connected through the drain 254 and the contact hole 424. The pad section 139 is electrically connected through the source 255 and the contact hole 425. The pad section 137 is

electrically connected with the gate electrode 253. The semiconductor layer 253 consists of a channel field, and the source field and drain field which have been arranged across a channel field. The gate insulator layer 2 is arranged so that the semiconductor layer 252 may be covered, the gate electrode 253 is arranged on the gate insulator layer 2, and TFT430 is formed. Semiconductor layer 256 portion which overlaps the gate electrode 253 superficially functions as a channel field. The drain field of the semiconductor layer 256 is electrically connected with the drain 254 through the contact hole 426. The source field of the semiconductor layer 256 is electrically connected with the source 255 through the contact hole 427. In measurement, a probe needle is contacted in the pad sections 137, 138, and 139 at each. Switching of TFT430 is turned on by impressing voltage to the pad section 137. The TFT property of TFT430 can be measured by applying voltage to the pad sections 138 and 139, measuring current, and converting into resistance. Thereby, the TFT property of N channel TFT160 of a shift register can be measured indirectly.

[0063] On the other hand, as shown in drawing 9 , in the field surrounded by the rectangle E of the P channel TFT test pattern 150, the pattern which measures the TFT property of TFT30 in a viewing area, and the pattern which measures the TFT property of P channel TFT140 of the shift register in a circumference drive circuit field are arranged.

[0064] The pattern which measures the TFT property of TFT in a viewing area The pad section 155, the pad section 156, the pad section 157, the gate electrode 263 formed in the same layer as the gate electrode of TFT30 in a viewing area, the drain 260 formed in the same layer as pixel electrode 9a in a viewing area, the source 261 formed in the same layer as the data line 6 in a viewing area, The gate insulator layer 2 which intervenes between the semiconductor layer 262 formed in the same layer as the semiconductor 1 of TFT30, and the semiconductor layer 262 and the gate electrode 263, It consists of an insulator layer 81, an insulator layer 4 between the 2nd layer, and an insulator layer 7 between the 3rd layer between the 1st layer which intervenes between the gate electrode 263 and a drain 260. As shown in drawing 9 , the drain 260 serves as a configuration which extended from the pad section 155. The pad section 156 is electrically connected through the source 261 and the contact hole 434. The pad section 157 is electrically connected with the gate electrode 263. The semiconductor layer 262 has LDD structure and consists of a channel field, the low concentration source field and low concentration drain field which have been arranged across a channel field, and the high concentration source field and high concentration drain field which have been arranged across these fields. The gate insulator layer 2 is arranged so that the semiconductor layer 262 may be covered, the gate electrode 263 is arranged on the gate insulator layer 2, and TFT440 is formed. Semiconductor layer 262 portion which overlaps the gate electrode 263 superficially functions as a channel field. The high concentration drain field of the semiconductor layer 262 is electrically connected with the drain 260 through the contact hole 439. The high concentration source field of the semiconductor layer 262 is electrically connected with the source 261 through the contact hole 434. In measurement, a probe needle is contacted in the pad sections 155, 156, and 157 at each. By impressing voltage to the pad section 157, the TFT property of TFT440 can be measured by turning on switching of TFT440, applying voltage to the pad sections 155 and 156, measuring current, and converting into resistance. Thereby, the TFT property of TFT30 in a viewing area can be measured indirectly.

[0065] The pattern which measures the TFT property of P channel TFT140 of the shift register in a circumference drive circuit field The source 265 formed in the same layer as the pad section 158, the pad section 157, the pad section 159, the gate electrode 263, the source electrode of N channel TFT140 of a shift resist, and a drain electrode and a drain 264, and the semiconductor layer of TFT of a shift resist and the semiconductor layer 266 of this layer, It consists of insulator layers 4 between the 2nd layer which intervenes between the gate insulator layer 2 which intervenes between the semiconductor layer 266 and the gate electrode 263 and the insulator layer 81 between the 1st layer, and the gate electrode 263, the source 265 and a drain 264. As shown in drawing 9 , the pad section 158 is electrically connected through the drain 264 and the contact hole 436. The pad section 159 is electrically connected through the source 265 and the contact hole 435. The pad section 157 is electrically connected with the gate electrode 263 through the contact hole 431. The semiconductor layer 266 consists of a channel field, and the source field and drain field which have been arranged across a channel field. The gate insulator layer 2 is arranged so that the semiconductor layer 266 may

be covered, the gate electrode 263 is arranged on the gate insulator layer 2, and TFT441 is formed. Semiconductor layer 266 portion which overlaps the gate electrode 263 superficially functions as a channel field. The drain field of the semiconductor layer 266 is electrically connected with the drain 264 through the contact hole 437. The source field of the semiconductor layer 266 is electrically connected with the source 265 through the contact hole 438. In measurement, a probe needle is contacted in the pad sections 157, 158, and 159 at each. Switching of TFT441 is turned on by impressing voltage to the pad section 157. The TFT property of TFT441 can be measured by applying voltage to the pad sections 158 and 159, measuring current, and converting into resistance. Thereby, the TFT property of P channel TFT140 of a shift register can be measured indirectly.

[0066] As mentioned above, as shown in drawing 8 and drawing 9 , the test pattern and the pad are arranged so that the probe card with which each test pattern is used at the time of the measurement in each test pattern may become common.

[0067] As mentioned above, in this operation gestalt, two or more different test patterns can be measured with a common probe card.

[0068] In addition, the test pattern for needless to say [that it is not what is limited to the test pattern indicated to **** as a test pattern] measuring the various element properties arranged on a substrate, the electrical property of the film itself which constitutes this element, etc. can be formed.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

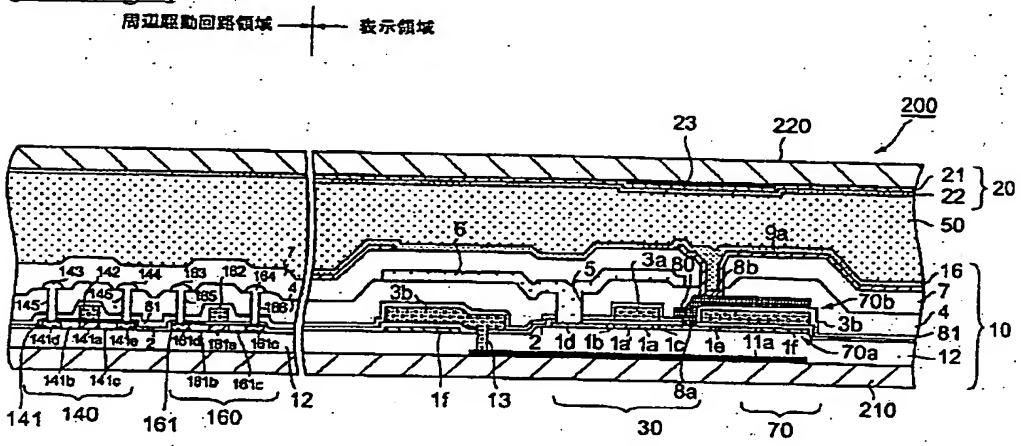
[Claim(s)]
[Claim 1] The manufacture method of an electrode substrate of providing the process which inspects the 1st test pattern of the above, and the 2nd test pattern of the above with the same probe card, respectively in the manufacture method of an electrode substrate of providing a substrate, the element arranged on the aforementioned substrate, the 1st test pattern which is arranged on the aforementioned substrate and measures the electrical property of the aforementioned element, and the 2nd test pattern which is arranged on the aforementioned substrate and measures the electrical property of the aforementioned element.
[Claim 2] It is the manufacture method of the electrode substrate according to claim 1 which the aforementioned element has N type TFT and P type TFT, and the 1st test pattern of the above is a test pattern which measures the electrical property of the aforementioned N type TFT, and is characterized by the 2nd test pattern of the above being a test pattern which measures the electrical property of the aforementioned P type TFT.
[Claim 3] The 1st test pattern of the above and the 2nd test pattern of the above are the manufacture method of the electrode substrate according to claim 1 or 2 characterized by having a probe needle corresponding to [have two or more pad sections arranged identically, respectively, and] the pad section of the aforementioned plurality [probe card / aforementioned].
[Claim 4] Substrate. The element arranged on the aforementioned substrate. The 1st test pattern which has two or more pad sections which are arranged on the aforementioned substrate and measure the electrical property of the aforementioned element. The 2nd test pattern which has two or more pad sections which are arranged on the aforementioned substrate and measure the electrical property of the aforementioned element. It is the electrode substrate equipped with the above, and two or more pad sections of the 1st test pattern of the above and each 2nd test pattern of the above are arranged, and it is characterized by the bird clapper so that a common probe card may be used for the aforementioned measurement of the 1st test pattern of the above, and each 2nd test pattern of the above.
[Claim 5] The electrode substrate according to claim 4 characterized by arrangement of two or more pad sections of the 1st test pattern of the above and each 2nd test pattern of the above being the same.
[Claim 6] It is the electrode substrate according to claim 4 or 5 which the aforementioned element has N type TFT and P type TFT, and the 1st test pattern of the above is a test pattern which measures the electrical property of the aforementioned N type TFT, and is characterized by the 2nd test pattern of the above being a test pattern which measures the electrical property of the aforementioned P type TFT.
[Claim 7] The electrode substrate manufactured by the manufacture method of an electrode substrate given in any 1 term of a claim 1 to the claim 3.
[Claim 8] Electro-optics equipment which has the electrode substrate of a publication in any 1 term of a claim 4 to the claim 7.

[Translation done.]

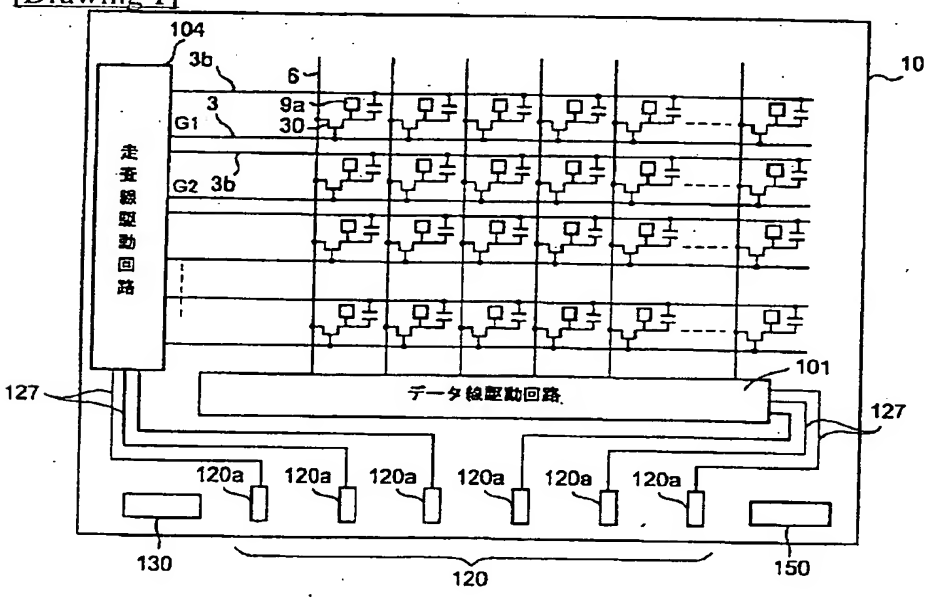
* NOTICES *

DRAWINGS

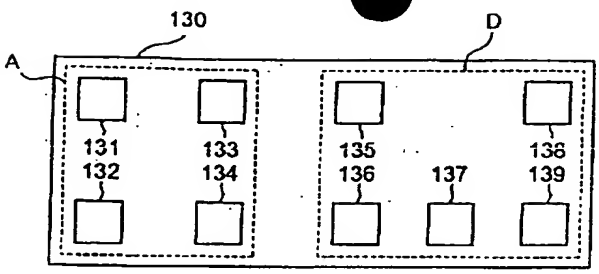
[Drawing 2]



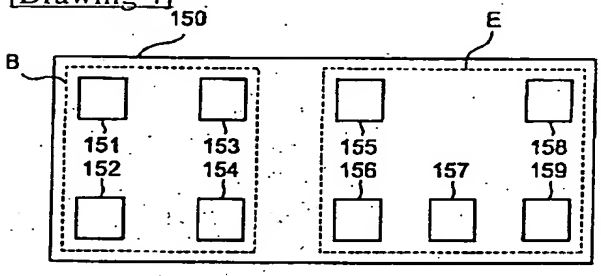
[Drawing 1]



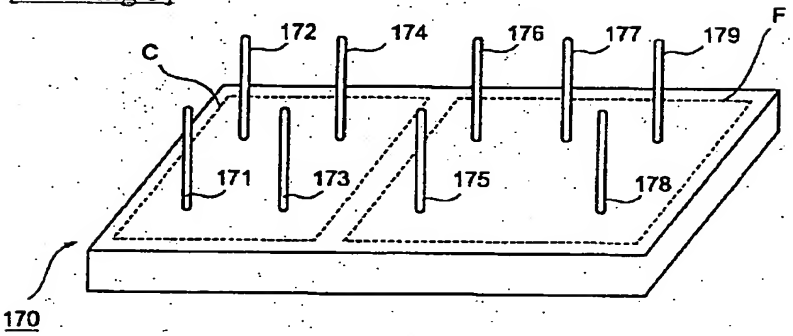
[Drawing 3]



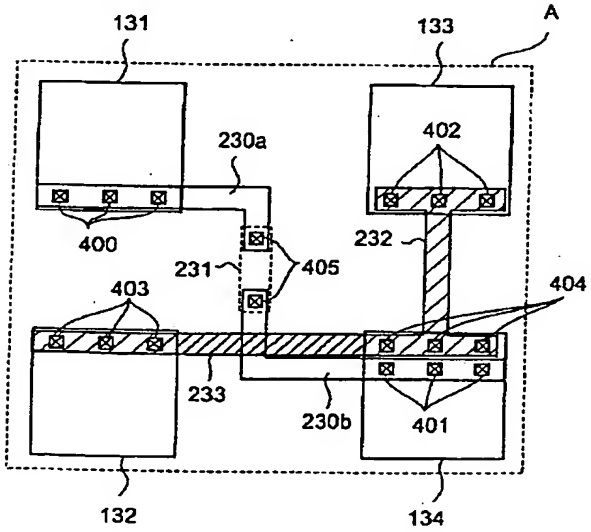
[Drawing 4]



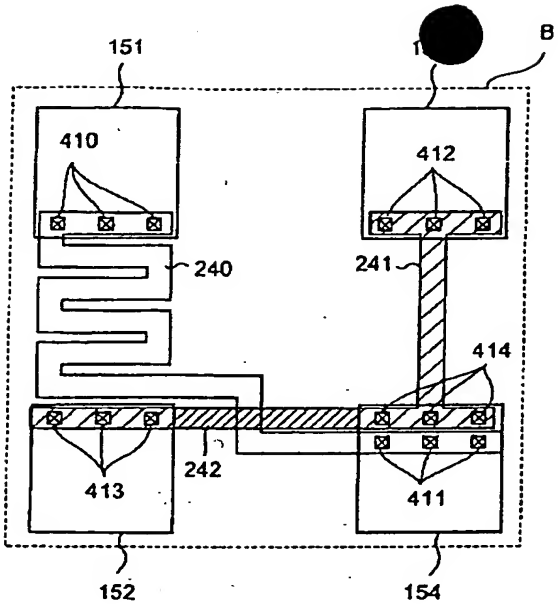
[Drawing 5]



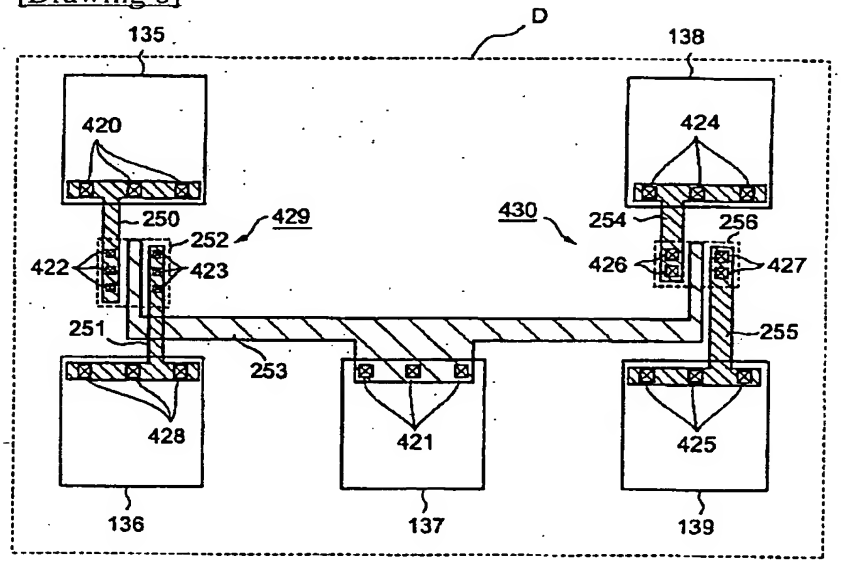
[Drawing 6]



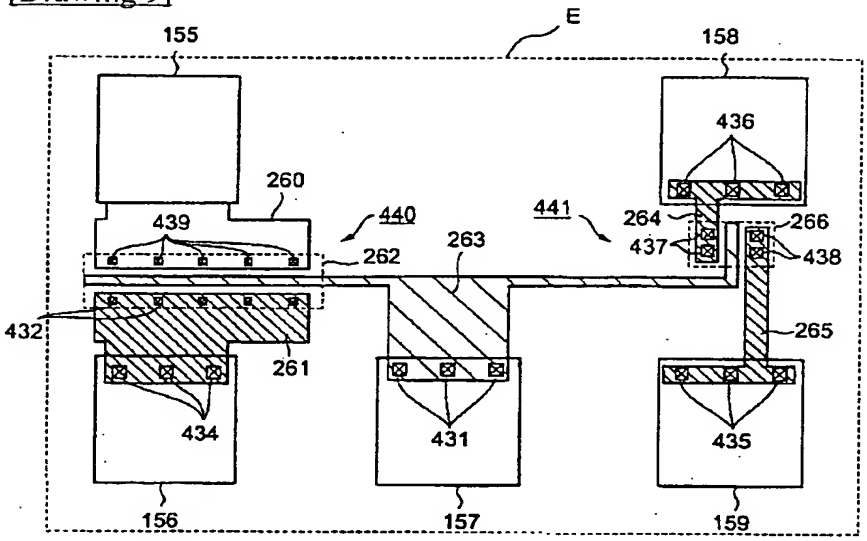
[Drawing 7]



[Drawing 8]



[Drawing 9]



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